UNITED STATES PATENT AND TRADEMARK OFFICE

A

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/706,154	11/03/2000	Marlo Nemirovsky	P3816	5008

23669 7590 07/28/2005

HUFFMAN LAW GROUP, P.C.
1832 N. CASCADE AVE.
COLORADO SPRINGS, CO 80907-7449

EXAMINER	
COLEMAN, ERIC	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 07/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/706,154	NEMIROVSKY ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 6-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4 and 6-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sharangpani (patent No. 5,699,537) in view of Hirata (patent No. 5,430,851).

3. Sharangpani taught the invention substantially as claimed including a data processing ("DP") system comprising:

a) Instruction cache (206,304) (e.g., see figs. 2, and 3) (or on chip memory or external memory subsystem in fig. 4)(e.g., see col. 4 line 63-col. 5 ,line 40);

b) Fetch logic (302, 402) coupled to the instruction cache enabled to concurrently fetch instructions from the instruction cache (e.g., see figs. 3,4 and col. 5, line 21-col. 7, line 61);

c) A plurality of instruction queues (322, 415,416,417,418) coupled to said fetch logic where each one of said plurality of instruction queues is associated with at least one instruction stream (e.g., see fig. 4);

d) A dispatch stage coupled to said plurality of instruction queues for selecting and dispatching instructions for said an instruction stream to a set of execution units [the instruction queue is part of the dispatch stage in fig 4 of Sharangpani and used for

dispatch of instructions by the dispatch stage and consequently would inherently be coupled to the instruction queues] (e.g., see col. 6, lines 28-64).

4. Sharangpani did not expressly detail (claims 1,7) that the instructions that were fetched concurrently were part of a plurality of threads. Hirata however taught the concurrent fetching of instruction for a plurality of threads (e.g., see fig. 2b where the three input arrow shows three inputs for streams of instructions from the cache to the instruction fetch unit and the three thread slots each comprising a separate program counter for keeping track of the instruction of the corresponding thread that was being fetched (e.g, see fig. 3 and col. 4, lines 50-col. 5, line 64).

5. It would have been obvious to one ordinary skill in the DP art to combine the teachings of Sharangpani and Hirata. Both references were directed toward the problems of fetching and providing instructions to plural execution units in parallel. One of ordinary skill in the art would have been motivated to incorporate the Hirata teachings of plural thread slot with individual program counters at least provide the Sharangpani with increased ablility to process complex programs as the incorporation of the Hirata teaching would have provided the combined system an efficient manner provide instructions to the execution units for to processing multithreaded programs.

6. Sharangpani did not expressly detail (claim 1,7) a select logic coupled to the instruction cache for selecting ones of the plurality of instruction streams to fetch instructions from the instruction cache. Sharangpani however taught fetching instruction from cache that are steered to plural distinct queues, each queue for providing instruction to a particular distinct type of execution unit (e.g., see fig. 4). From this the

fetch unit fetches the instructions for the different type of execution units. Also Sharangpani taught branch execution logic and branch prediction logic for fetching instructions from cache (e.g,. see fig. 4) the branch micro-pipeline is taught as affects the operation of the execution front end in fetching and execution instructions down the correct path of the branch. Therefore it would have been obvious to one of ordinary skill that in at least one implementation of the Sharagpani teachings the system comprised select logic coupled to the instruction cache for selecting ones of the plurality of instruction streams to fetch instructions from the instruction cache. This is apparent also because since the fetching is for plural streams selection of instructions for each stream would have been required. Further (as to claims 1,2,4,7,8) One of ordinary skill would have been motivated to provide for the selection of streams to fetch so that if one stream did not have any more instructions in the cache then the system would not waste time in trying to receive fetch requests from a stream that had no further instructions in the cache although it may have instructions in its queue. In this case the number of stream being fetched from would have been less than the number of instruction streams executing. On the other hand the Thread slot logic of figure 2a with individual program counters in Hirata collectively provided selection of instruction streams to be fetched by Hirata.

7. As per claim 3,9,10 since the Sharangpani and Hirata execute plural streams at the same time plural program counters would have been required to keep track of where in each stream the execution unit were executing so that the correct next instruction could be fetched (e.g., see fig. 3 of Sharangpani and fig 2a of Hirata).

8. As per claim 6, Sharangpani taught the fetch logic concurrently storing instructions into ones of said plurality of instruction queues that would be associated in the combined system with said ones of said plurality of instruction streams by said fetch logic ((e.g., see fig. 4 and col. 8, line 12-col. 9, line 56).

9. As per claim 11, Sharangpani taught dispatching stage logic for dispatching instructions to a plurality of execution units (e.g., see fig.4 and col. 6, lines 36-66).

10. As per claim 12, Sharangpani did not expressly detail the plurality of execution units comprises eight arithmetic logic units (ALUs) and two memory units. Hirata taught eight units comprising two load store units and six functional units (see fig. 2a). The implementation in the embodiment detailed by Sharangpani using four execution units would not have prevented modification in the implementation of the Sharangpani teachings by expansion of the system to incorporate any reasonable number of execution units. The particular number of execution units in the range of ten would not be beyond mere the level of skill of one of ordinary skill to implement using the teachings of Sharapani and HIrata. Further the connection to two memory unit especially since the Sharangpani system comprised load/store unit would have been within the level of skill of one of ordinary skill in the art considering the Sharangpani teachings to implement. The motivation to implement the system in that manner comes from the applications that would be implemented and the Examiner contends that a application for processing multiple streams of search queries such as via as would be used in a search engine would have motivated one of ordinary skill to expand the Sharangpani system to incorporate ten processors and two memories.

Response to Arguments

11. Applicant's arguments with respect to claims 1-4 and 6-12 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Joshi (patent No. 5,604,909) disclosed a system for processing instruction using plural instruction queue for queuing instruction to be sent to function units (e.g., see abstract and figs. 3,5).

Corwin (patent No. 6,378,063) disclosed a system for routing dependent claims to clustered instruction units and uses queue to queue instructions to be dispatched to clustered execution units (e.g., see fig. 2).

Olson (patent No. 6,622,240) disclosed a system with parallel connections between cache memory and fetch unit (e.g. see fig. 1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC

ERIC COLEMAN
PRIMARY EXAMINER